IN THE CLAIMS

1. (Currently amended) A charge detection device comprising:

a floating diffusion;

a feed through shielding transistor coupled to the floating diffusion;

a reset transistor coupled to the shielding transistor;

an output diode diffusion coupled to the reset transistor;

a bias tracking voltage reference generator coupled to the output diode diffusion for providing bias to the output diode diffusion; and

wherein an input of the reference generator is coupled to a gate of the feed through shielding transistor.

2. (Original) The device of claim 1 wherein the gate of the feed through shielding transistor overlaps a gate of the reset transistor.

3. (Original) The device of claim 1 wherein a fixed amount of charge is kept under the gate of the feed through shielding transistor to provide a reset time constant.

4. (Currently amended) The device of claim 1 wherein a low-doped region surrounds the floating diffusion [[region]] and is adjacent

to the gate of the feed through shielding transistor for the purpose of minimizing the gate to n+ overlap capacitance.

5. (Original) The device of claim 1 wherein the floating diffusion is an n+ diffusion region.

6. (Original) The device of claim 5 wherein a low-doped n type region surrounds the n+ floating diffusion region and is adjacent to the gate of the feed through shielding transistor for the purpose of minimizing the gate to n+ overlap capacitance.

7. (Currently amended) The device of claim 1 wherein the voltage reference generator comprises a transistor that is equivalent to the [[reset-]] feed through shielding transistor.

8. (Original) The device of claim 7 wherein a predetermined amount of charge is maintained in a channel of the reset-shielding transistor after a reset has been made, independent of process parameter variations and gate bias variations.